



Compact Modeling of Cryogenic CMOS Circuits Using Verilog-A

Akin Akturk^{†‡}, Siddharth Potbhare^{†‡}, Marty Peckerar[†], Mahsa Dornajafi[†], Zeynep Dilli[†] and Neil Goldman^{†‡}

[†]Department of Electrical and Computer Engineering
University of Maryland
College Park, MD 20742

[‡]CoolCAD Electronics
Takoma Park, MD 20912

K. Eng, R. Young, E. Longoria, T. Gurrieri, J. Levy and M. S. Carroll

Sandia National Laboratories
Albuquerque, NM, 87185

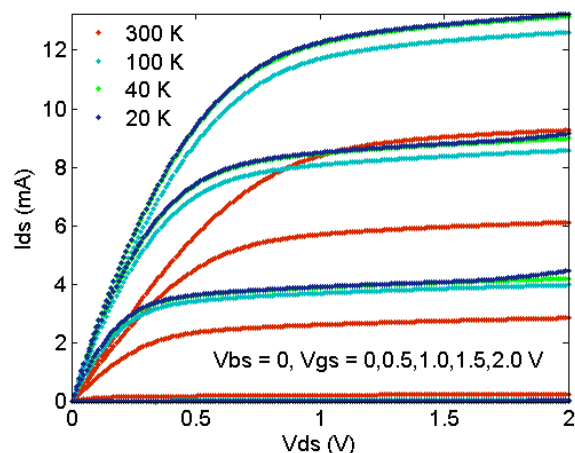


Objectives and Outline

Program Objectives

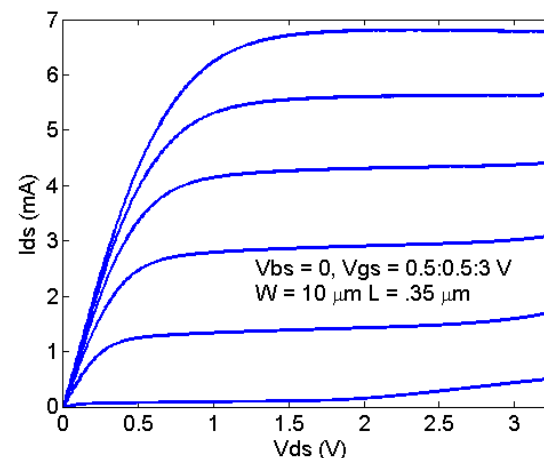
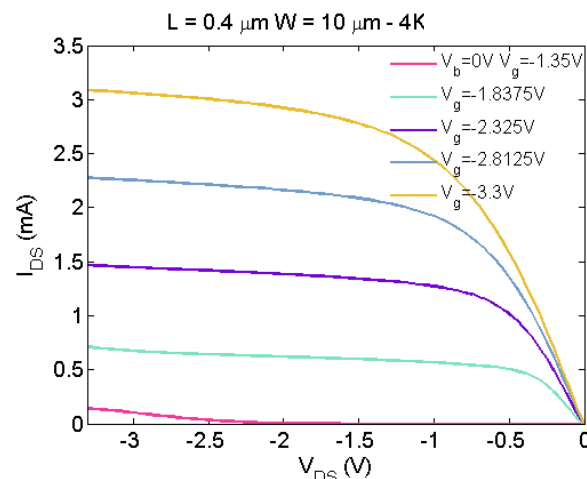
- *To develop a formalism that is adaptable to our current state-of-the-art modeling tools (SPICE, Cadence, BSIM, Synopsis, etc.)*
- *To improve our understanding of carrier transport in component structures at low temperature*
- Do MOSFETs work much below 77K – the carriers freeze out? What gives?
 - Impurity band formation
 - Mobile channel densities and space charge
- The nitty-gritty
 - Temperature dependent device / compact model parameters
 - Temperature-dependent effects: Incomplete ionization, possible self-heating, impact ionization, intrinsic carrier concentration variations
- Results and Conclusions

What do MOSFET IV Curves Look Like At Low Temperature?



Temperature-Dependent I-V Curves of a 0.16 μm NMOS

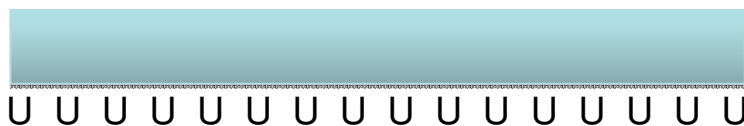
$W = 15.6 \mu\text{m}$ $L = 0.16 \mu\text{m}$
Bulk Lucent NMOSFET



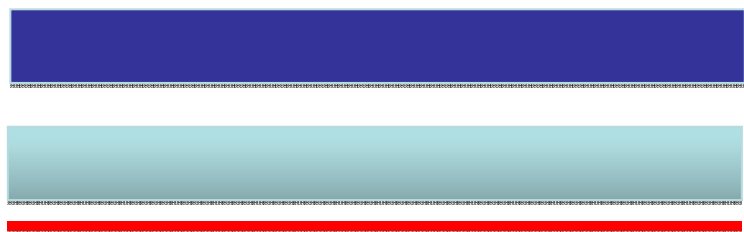
4 K I-V Curves of CMOS7 NMOS/PMOS

PRETTY MUCH LIKE THEY DO AT ROOM TEMPERATURE!

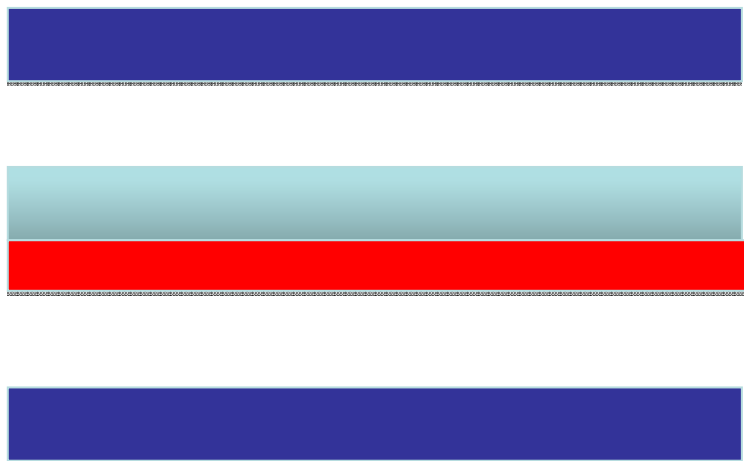
The Impurity Band Model*



A. Discrete States



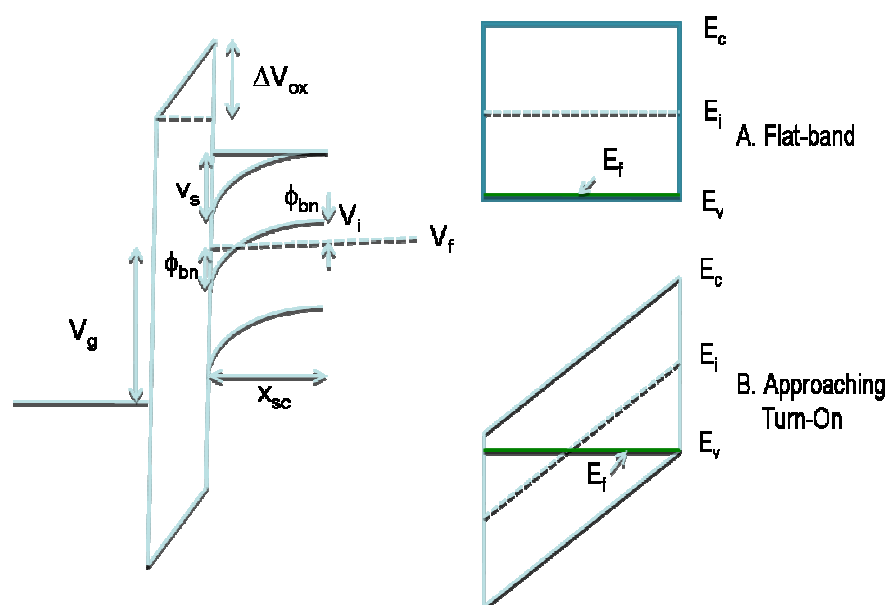
B. On-set of impurity band formation



C. Broadening of the impurity band and overlap with the main band

*Esther Conwell, "Impurity Band Formation In Germanium and Silicon," Phys. Rev. **103**(1),51(1956)

The Zero-Order Turn-On Model



- Oxide thickness is negligible
- No fixed charge in either the oxide or in the bulk
- $V_{th}^0 = 1.15V$
- What do we observe?
 - $V_{th} = 1.35V$ (p-channel)
 - $V_{th} = 0.95V$ (n-channel)



Compact Modeling using Verilog-A Behavioral Language

Develop a formalism that is adaptable to our current state-of-the-art modeling tools (SPICE, Cadence, BSIM, Synopsis, etc.)

Compact Modeling of Extreme Environment Electronics

Aiding development / design of extreme low temperature integrated circuits !

- Compact models are necessary to efficiently simulate large size integrated circuits to achieve first-pass designs.
- Most commonly used compact model in industry is BSIM (BSIM3, BSIM4, BSIMSOI)
- BSIM is comprised of MANY analytical equations. Along with approximately 400 model parameters, it is used to simulate MOSFET current-voltage curves.

For example, threshold voltage calculation in BSIM3 is shown on the right.

$$\begin{aligned}
 V_{th} = & V_{th0ox} + K_{1ox} \cdot \sqrt{\Phi_s - V_{bseff}} - K_{2ox} V_{bseff} \\
 & + K_{1ox} \left(\sqrt{1 + \frac{N_A x}{L_{eff}}} - 1 \right) \sqrt{\Phi_s} + (K_3 + K_{3b} V_{bseff}) \frac{T_{ox}}{W_{eff} + W_0} \Phi_s \\
 & - D_{VT0w} \left(\exp \left(-D_{VT1w} \frac{W_{eff}' L_{eff}}{2 l_{tw}} \right) + 2 \exp \left(-D_{VT1w} \frac{W_{eff}' L_{eff}}{l_{tw}} \right) \right) (V_{bi} - \Phi_s) \\
 & - D_{VT0} \left(\exp \left(-D_{VT1} \frac{L_{eff}}{2 l_t} \right) + 2 \exp \left(-D_{VT1} \frac{L_{eff}}{l_t} \right) \right) (V_{bi} - \Phi_s) \\
 & - \left(\exp \left(-D_{sub} \frac{L_{eff}}{2 l_{to}} \right) + 2 \exp \left(-D_{sub} \frac{L_{eff}}{l_{to}} \right) \right) (E_{tso} + E_{tso} V_{bseff}) V_{ds}
 \end{aligned}$$

Compact BSIM Models

- Advantages:

It is fast! There are many commercial simulators that efficiently solve BSIM equations.

A tremendous knowledge base on device operation is already established.

- Disadvantages:

BSIM simulation results can be adjusted only by changing device model parameters (User is not allowed to see/access/modify BSIM equations).

BSIM model is developed for modeling MOSFETs operating approximately in the 250 – 450 K temperature range.

BSIM I-V curves deviate from measurements at extreme low temperatures.

There is no explicit way to incorporate incomplete ionization effects.

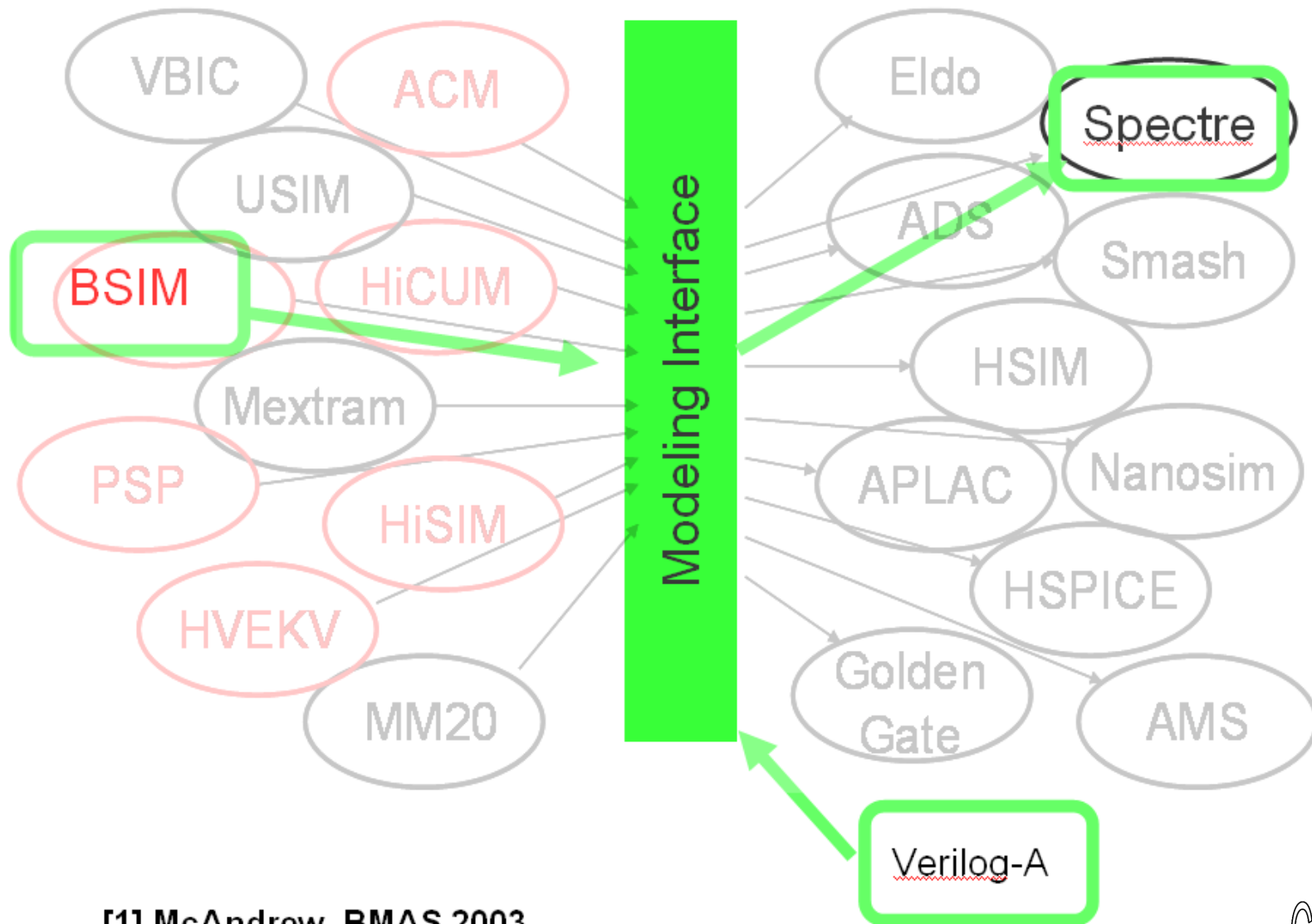
BSIM has too many parameters!

Development of cryogenic integrated circuits !

Goal is to take advantage of the simulators / model parameter extractors and modeling experience coming with the use of a BSIM model but at the same time tailor its equation and parameter lists to be able to resolve extreme environment operation.

SOLUTION: Use Verilog-A along with BSIM equations and parameters, and incorporate temperature specific effects by modifying equations and parameters in Verilog-A!

A Solution to Automated Cryogenic Design



[1] McAndrew, BMAS 2003

Cryogenic Design Suite

Compact Models / Analytical Equations

BSIM

BSIM is a set of analytical equations for describing MOSFET operation. Only model parameters are user accessible!

Verilog-A

Parameters as well as equations are user-defined and can be modified at any time.

**Spectre
ADS
SmartSpice
HSPICE...**

BSIM and Verilog-A need a compiler and a solver.

Calculated I-V Curves

Detailed Distributed Device Modeling

Device Simulator

Verilog-A

- Verilog-A = Analog Hardware Description / Behavioral Modeling Language
- Verilog-A runs in almost all commercial device simulators = Cadence Spectre, Agilent ADS, Silvaco Smartspice
 - **Very portable!**
 - **Unlike BSIM type compact models Verilog-A codes are transparent enabling change of parameter lists as well as equations!**
- Takes advantage of the built-in matrix solver of the simulation program it is running in.
- Fully integrated with other simulation programs within the simulator. For example, part of the circuit can be modeled in Verilog-a and the rest in BSIM.
- Verilog-A language is relatively simple to understand and simulators allow users change the code.

We use BSIM3/4 translated into Verilog-A language. Therefore, we have access to BSIM3/4 model parameters as well as equations.

Example Verilog-A Code

```
module mosfet(drain, gate, source, bulk);  
    inout drain, gate, source, bulk;  
    electrical drain, gate, source, bulk;  
    electrical drainp, sourcep; // internal nodes  
`ifdef NQSMOD  
    electrical q;           // NQS charge model node  
`endif
```

```
    //***** Device Parameters *****/
```

```
    parameter real L      = 5.0e-6;
```

```
    parameter real W      = 5.0e-6;
```

```
    .....
```

```
vbs = TYPE * V(bulk, sourcep);
```

```
vgs = TYPE * V(gate, sourcep);
```

```
    .....
```

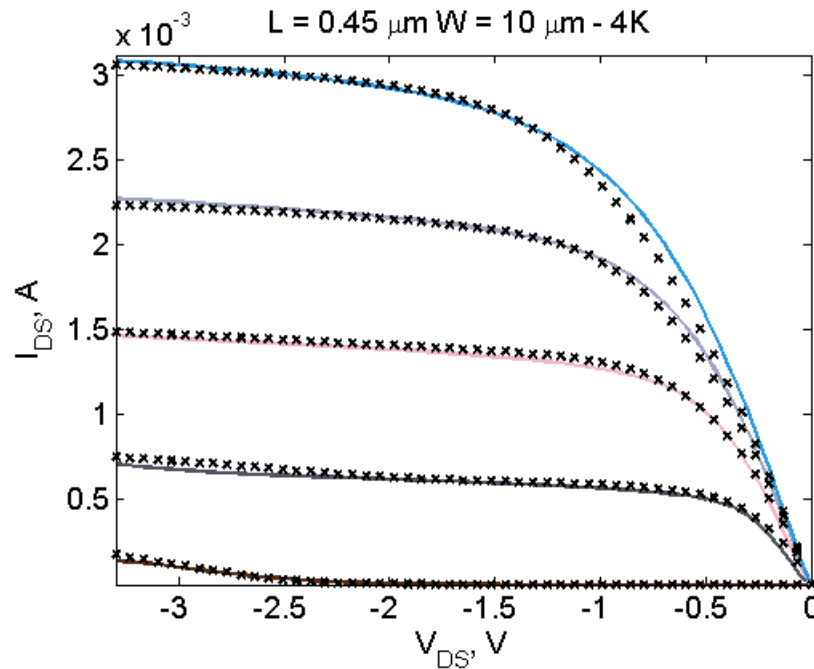
```
I(gate) <+ TYPE * (-1) * qdef * gtau;
```

```
I(drainp) <+ TYPE * dxpart * qdef * gtau;
```

*BSIM3 Verilog-A code is
approximately 6000 lines!*

4 K CMOS7 Verilog-A Simulations vs. Measurements

BSIM4 model parameters as well as equations are adjusted.



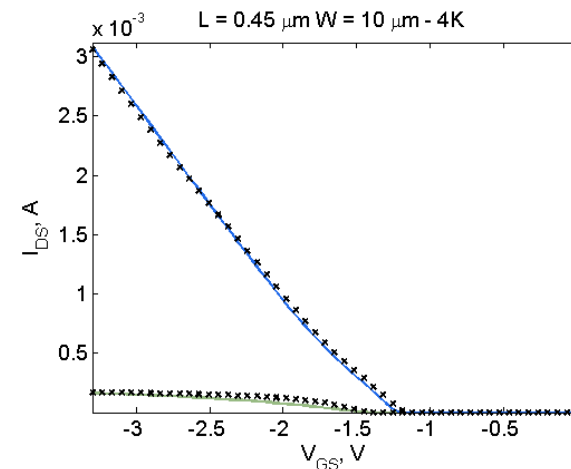
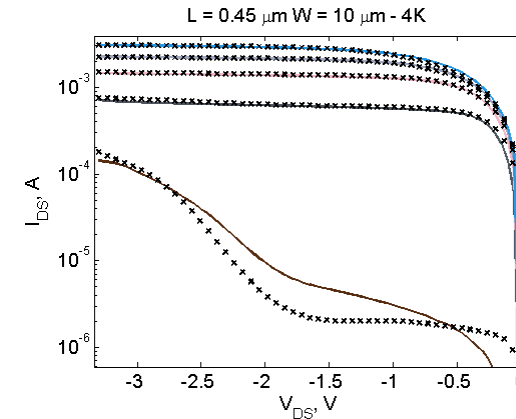
$V_{GS} = -1.35, -1.8375, -2.325, -2.8125, -3.3 \text{ V}$

$V_{BS} = 0 \text{ V}$

PSOI

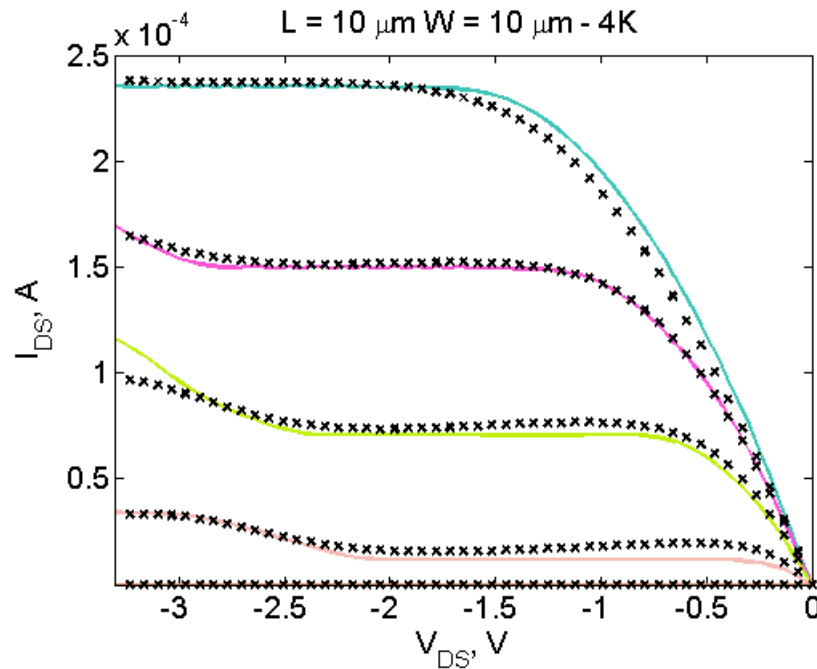
Symbols: Simulations

Solid lines: Measurements



4 K CMOS7 Verilog-A Simulations vs. Measurements

BSIM4 model parameters as well as equations are adjusted.



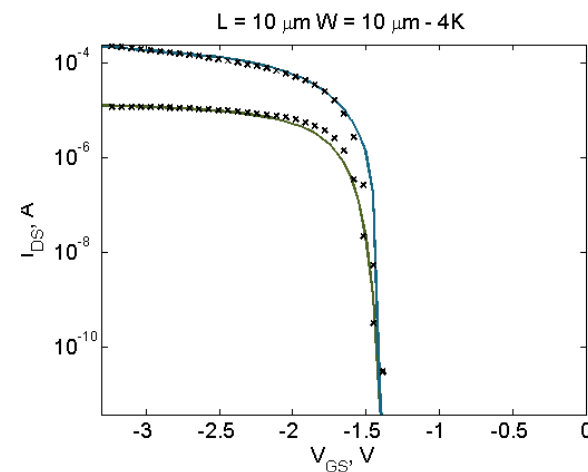
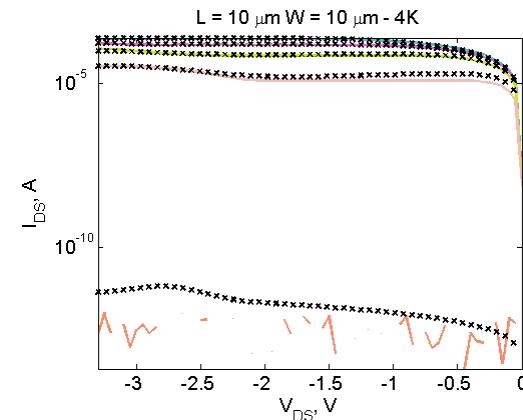
$V_{GS} = -1.35, -1.8375, -2.325, -2.8125, -3.3 \text{ V}$

$V_{BS} = 0 \text{ V}$

PSOI

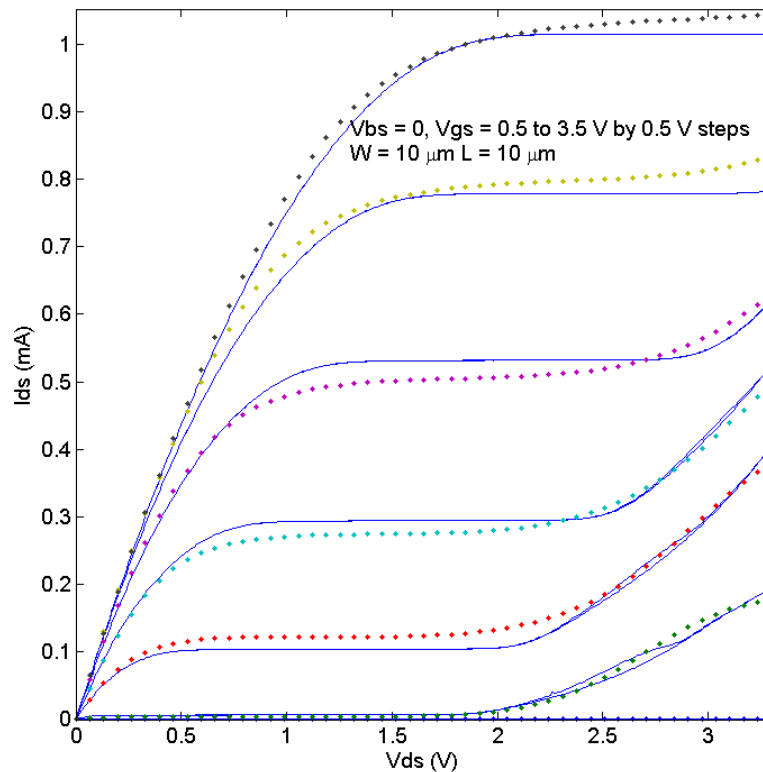
Symbols: Simulations

Solid lines: Measurements



4 K CMOS7 Verilog-A Simulations vs. Measurements

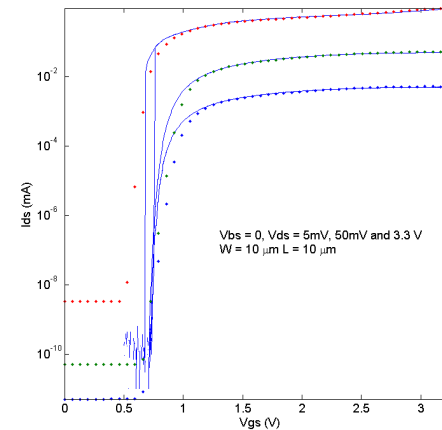
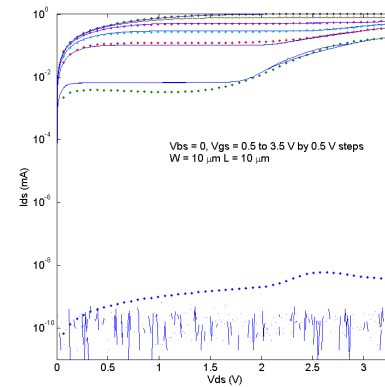
BSIM4 model parameters as well as equations are adjusted.



NSOI

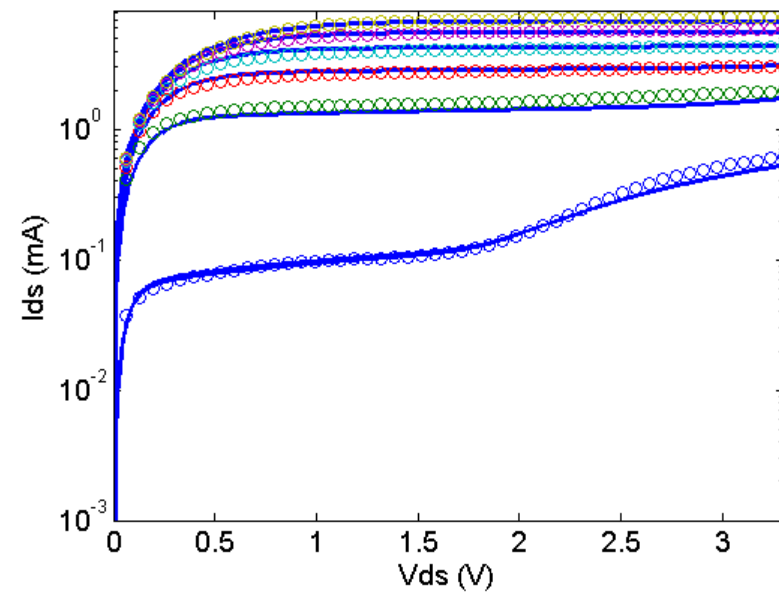
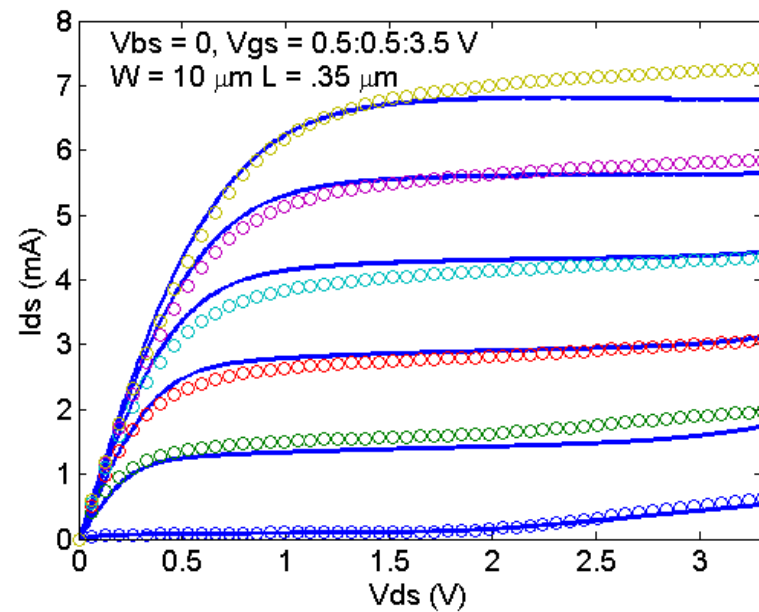
Symbols: Simulations

Solid lines: Measurements



4 K CMOS7 Verilog-A Simulations vs. Measurements

BSIM4 model parameters as well as equations are adjusted.

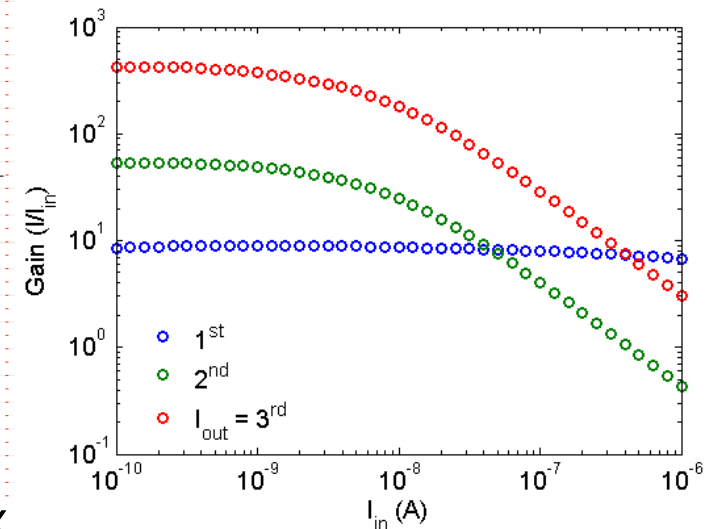
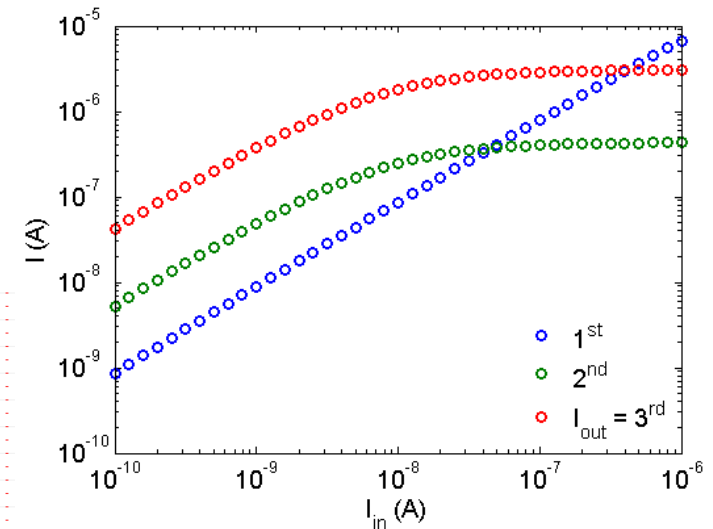
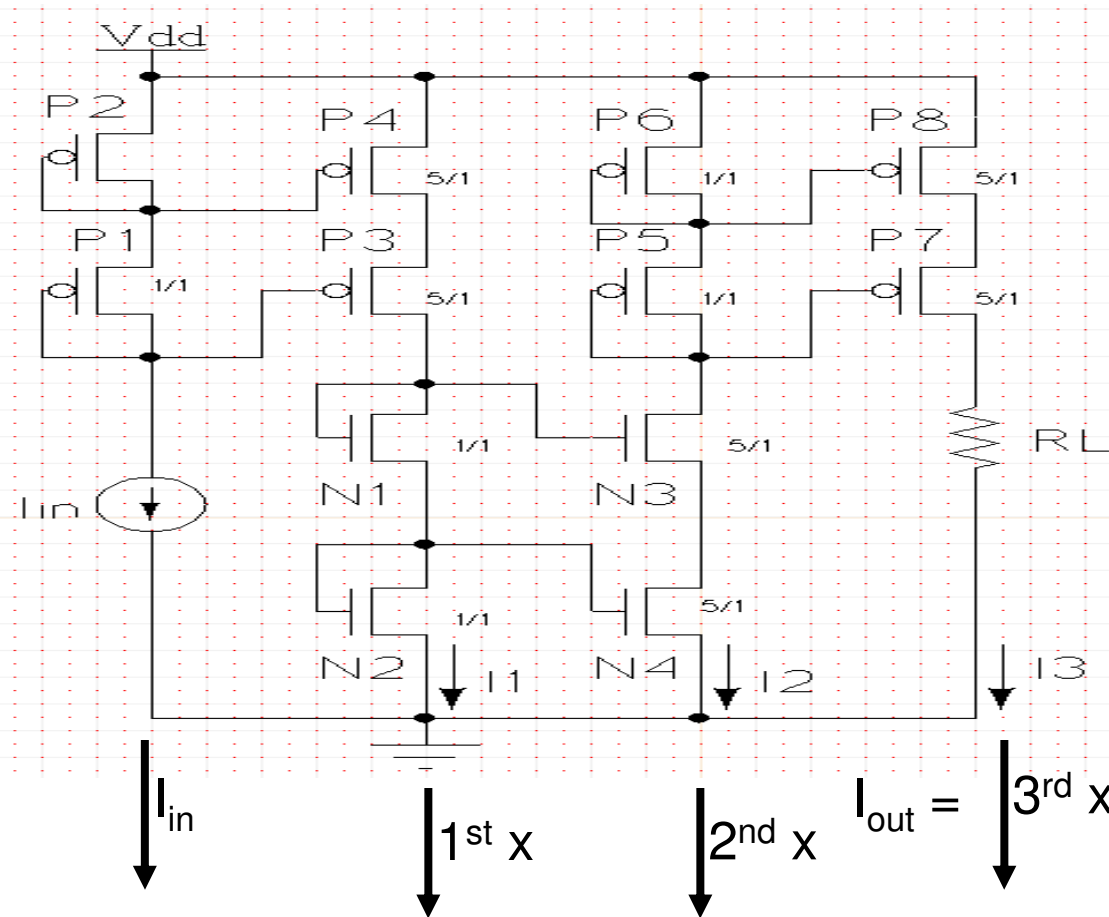
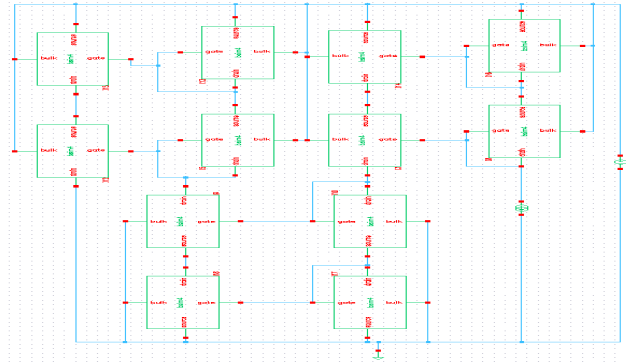


NSOI

Symbols: Simulations

Solid lines: Measurements

4 K Compact Modeling BSIM4 Verilog-A: Current Amplifier



Conclusion

- MOSFET devices exhibit different physical effects at low temperatures.
- To be able to use BSIM-type compact models at low temperatures, we change model parameters as well as equations.
- Using the Verilog-A BSIM approach, we successfully matched the measured and calculated IV curves of NMOS/PMOS devices with varying W/Ls.
- We also developed a compact model library universal for all the tested MOSFETs.
- We believe that incomplete and impact ionizations play an important role at cryogenic temperatures, although they are typically not significant at room temperature.
 - Especially at low gate biases, the IV curves display very non-linear characteristics, which must be modeled.
 - At high frequencies, freeze-out affects frequency response.
 - We are currently investigating appropriate models for low-temperature operation.
- Low temperatures and the resulting extremely low intrinsic carrier concentrations make low temperature device simulations very challenging. (Convergence also takes a long time.) However, so far we have made good progress on addressing many numerical issues.